



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of Clive M. Philbrick et al.

Ser. No: 09/802,551

Filing Date: March 9, 2001

Examiner: Chang Jungwon

Atty. Docket No: ALA-012

GAU: 2154

For: INTELLIGENT NETWORK STORAGE INTERFACE SYSTEM

February 27, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

10th Supplemental Information Disclosure Statement per 37 C.F.R. §1.98

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicants bring thirty-three documents to the attention of the Examiner in the above-identified application. Enclosed are copies of fourteen non-Patent reference documents listed on the enclosed one-page form PTO-1449. Copies of the nineteen U.S. Patent documents are not enclosed. Many of these documents were previously submitted, however, these documents were submitted in a Information Disclosure Statement after a final rejection and may have not been considered.

Because prosecution has been reopened with a non-final Office Action, applicants are submitting the referenced documents for consideration by the Examiner under 37 C.F.R. § 1.97(c)(2) along with the requisite fee of \$180.00.

Citation of these documents shall not be construed as an admission that the documents are prior art with respect to the instant invention, a representation that a search has been made, or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

CERTIFICATE OF MAILING

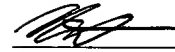
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on February 27, 2006.

Date: 2-27-06

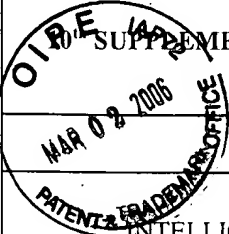


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Respectfully submitted,



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U.S. Department of Commerce, Patent and Trademark Office		Application No.: 09/802,551
 <p>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p>		Filing date: March 9, 2001
		Inventors: Clive M. Philbrick et al.
		Group Art Unit: 2154
		Examiner name: Chang Jungwon
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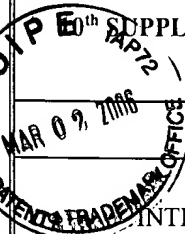
U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	1	2001/0004354	01/10/01	Jolitz	370	328	
	2	4,589,063	5/13/86	Shah et al.	710	8	
	3	5,524,250	6/4/96	Chesson et al.	395	775	
	4	5,592,622	1/7/97	Isfeld et al.	395	200.02	
	5	5,619,650	4/8/97	Bach et al.	395	200.01	
	6	5,727,142	3/10/98	Chen	395	181	
	7	5,778,013	7/7/98	Jedwab	714	807	
	8	5,802,258	9/1/98	Chen	395	182.08	
	9	5,898,713	4/27/99	Melzer et al.	371	53	
	10	5,970,804	10/26/99	Osborne	395	200.75	
	11	6,021,507	2/1/00	Chen	714	2	
	12	6,038,562	3/14/00	Anjur et al.	707	10	
	13	6,047,323	4/4/00	Krause	709	227	
	14	6,067,569	5/23/00	Khaki et al.	709	224	
	15	6,070,200	5/30/00	Gates et al.	710	20	
	16	6,101,555	8/8/00	Goshey et al.	709	321	
	17	6,145,017	11/7/00	Ghaffari	710	5	
	18	6,157,955	12/5/00	Narad et al.	709	228	
	19	6,172,980	1/9/01	Flanders et al.	370	401	
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Examiner

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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OTHER ART—NON PATENT LITERATURE DOCUMENTS

*Examiner Initial		(Including Author, Title, Date, Pertinent Pages, Etc.)
	1	Beach, Bob, IEEE Computer Society Press publication entitled, "UltraNet: An Architecture for Gigabit Networking", from 15 th Conference on Local Computer Networks, 18 pages, Sept. 30 – Oct. 3, 1990.
	2	Chesson et al., IEEE Symposium Record entitled, "The Protocol Engine Chipset", from Hot Chips III, 16 pages, Aug. 26-27, 1991.
	3	Intel article entitled "Solving Server Bottlenecks with Intel Server Adapters", Copyright Intel Corporation, 1999, 8 pages.
	4	Koufopavlou et al., IEEE Global Telecommunications Conference, Globecom '92, presentation entitled, "Parallel TCP for High Performance Communication Subsystems", 7 pages, Dec. 6-9, 1992.
	5	Lilienkamp et al., Publication entitled "Proposed Host-Front End Protocol", 56 pages, Dec. 1984.
	6	Macleane et al., IEEE Global Telecommunications Conference, Globecom '91, presentation entitled, "An Outboard Processor for High Performance Implementation of Transport Layer Protocols", 7 pages, Dec. 2-5, 1991.
	7	Publication entitled "Protocol Engine Handbook", 44 pages, Oct. 1990.
	8	Ross et al., IEEE article entitled "FX1000: A high performance single chip Gigabit Ethernet NIC", from Compcon '97 Proceedings, 7 pages, Feb. 23-26, 1997.
	9	Schwaderer et al., IEEE Computer Society Press publication entitled, "XTP in VLSI Protocol Decomposition for ASIC Implementation", from 15 th Conference on Local Computer Networks, 5 pages, Sept. 30 – Oct. 3, 1990.
	10	Strayer et al., "Ch. 9: The Protocol Engine" from XTP: The Transfer Protocol, 12 pages, July 1992.
	11	Thia, Y.H. Publication entitled "High-Speed OSI Protocol Bypass Algorithm with Window Flow Control", <u>Protocols for High Speed Networks</u> , pages 53-68, 1993.
	12	Thia, Y.H. Publication entitled "A Reduced Operational Protocol Engine (ROPE) for a multiple-layer bypass architecture", <u>Protocols for High Speed Networks</u> , pages 224-239, 1995.
	13	WindRiver article entitled "Tornado: For Intelligent Network Acceleration", copyright Wind River Systems, 2001, 2 pages.
	14	WindRiver White Paper entitled "Complete TCP/IP Offload for High-Speed Ethernet Networks", Copyright Wind River Systems, 2002, 7 pages.
Examiner	Date Considered	

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